

MAXIM

10-Bit Bus LVDS Serializers

MAX9205/MAX9207

General Description

The MAX9205/MAX9207 serializers transform 10-bit-wide parallel LVCMOS/LVTTL data into a serial high-speed bus low-voltage differential signaling (LVDS) data stream. The serializers typically pair with deserializers like the MAX9206*/MAX9208*, which receive the serial output and transform it back to 10-bit-wide parallel data.

The MAX9205/MAX9207 transmit serial data at speeds up to 400Mbps and 660Mbps, respectively, over PC board traces or twisted-pair cables. Since the clock is recovered from the serial data stream, clock-to-data and data-to-data skew that would be present with a parallel bus are eliminated.

The serializers require no external components and few control signals. The input data strobe edge is selected by TCLK_R/F. PWRDN is used to save power when the devices are not in use. Upon power-up, a synchronization mode is activated, which is controlled by two SYNC inputs, SYNC1 and SYNC2.

The MAX9205 can lock to a 16MHz to 40MHz system clock, while the MAX9207 can lock to a 40MHz to 66MHz system clock. The serializer output is held in high impedance until the device is fully locked to the local system clock, or when the device is in power-down mode.

Both the devices operate from a single +3.3V supply, are specified for operation from -40°C to +85°C, and are available in 28-pin SSOP packages.

Applications

- | | |
|------------------------------|------------------------------|
| Cellular Phone Base Stations | DSLAMs |
| Add Drop Muxes | Network Switches and Routers |
| Digital Cross-Connects | Backplane Interconnect |

Features

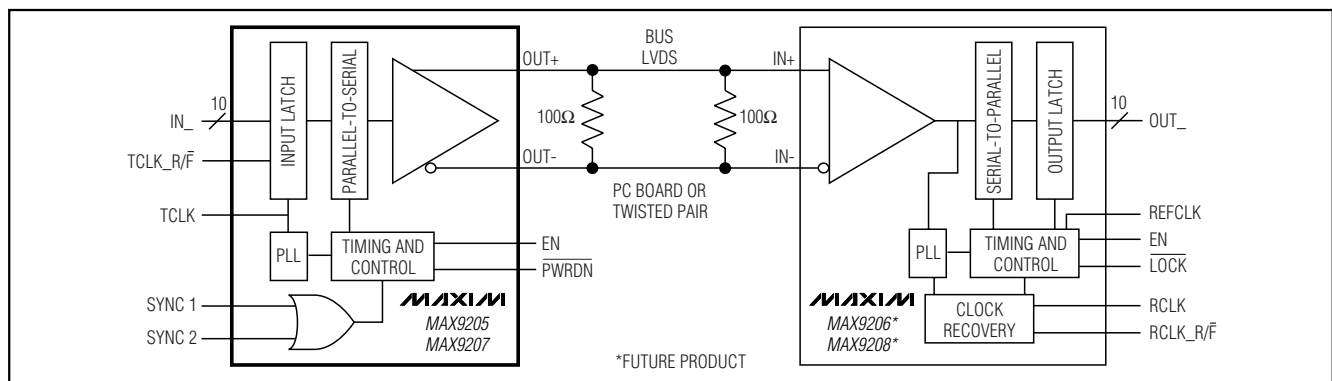
- ◆ Standalone Serializer (vs. SERDES) Ideal for Unidirectional Links
- ◆ Framing Bits for Deserializer Resync Allow Hot Insertion Without System Interruption
- ◆ LVDS Serial Output Rated for Point-to-Point and Bus Applications
- ◆ Wide Reference Clock Input Range
16MHz to 40MHz (MAX9205)
40MHz to 66MHz (MAX9207)
- ◆ Low 140ps (pk-pk) Deterministic Jitter (MAX9207)
- ◆ Low 34mA Supply Current (MAX9205)
- ◆ 10-Bit Parallel LVCMOS/LVTTL Interface
- ◆ Up to 660Mbps Payload Data Rate (MAX9207)
- ◆ Programmable Active Edge on Input Latch
- ◆ Pin-Compatible Upgrades to DS92LV1021 and DS92LV1023

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	REF CLOCK RANGE (MHz)
MAX9205EAI	-40°C to +85°C	28 SSOP	16 to 40
MAX9207EAI	-40°C to +85°C	28 SSOP	40 to 66

Pin Configuration and Functional Diagram appear at end of data sheet.

Typical Application Circuit



*Future product—contact factory for availability.

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ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND-0.3V to +4.0V
 IN₋, SYNC1, SYNC2, EN, TCLK_R/F, TCLK,
 PWRDN to GND.....-0.3V to (V_{CC} + 0.3V)
 OUT+, OUT- to GND-0.3V to +4.0V
 Output Short-Circuit Duration.....Continuous
 Continuous Power Dissipation (T_A = +70°C)
 28-Pin SSOP (derate 9.5mW/°C above +70°C)762mW

Storage Temperature Range-65°C to +150°C
 Junction Temperature+150°C
 Operating Temperature Range-40°C to +85°C
 Lead Temperature (soldering, 10s)+300°C
 ESD Protection (Human Body Model, OUT+, OUT-)±8kV

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, R_L = 27Ω ±1% or 50Ω ±1%, C_L = 10pF, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V and T_A = +25°C, unless otherwise noted.) (Notes 1, 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LVCNOS/LVTLL LOGIC INPUTS (IN0 TO IN9, EN, SYNC1, SYNC2, TCLK, TCLK_R/F, PWRDN)							
High-Level Input Voltage	V _{IH}			2.0		V _{CC}	V
Low-Level Input Voltage	V _{IL}			GND		0.8	V
Input Current	I _{IN}	V _{IN-} = 0 or V _{CC}		-20		+20	μA
BUS LVDS OUTPUTS (OUT+, OUT-)							
Differential Output Voltage	V _{OD}	Figure 1	R _L = 27Ω	200	286	400	mV
			R _L = 50Ω	250	460	600	mV
Change in V _{OD} Between Complementary Output States	ΔV _{OD}	Figure 1			1	35	mV
Output Offset Voltage	V _{OS}	Figure 1		0.9	1.15	1.3	V
Change in V _{OS} Between Complementary Output States	ΔV _{OS}	Figure 1			3	35	mV
Output Short-Circuit Current	I _{OS}	OUT+ or OUT- = 0, IN0 to IN9 = PWRDN = EN = high			-13	-15	mA
Output High-Impedance Current	I _{OZ}	PWRDN or EN = 0.8V, OUT+ or OUT- = 0 or V _{CC}		-10		+10	μA
Power-Off Output Current	I _{OX}	V _{CC} = 0, OUT+ or OUT- = 0 or 3.6V		-10		+10	μA
POWER SUPPLY							
Supply Current	I _{CC}	R _L = 27Ω or 50Ω worst-case pattern (Figures 2, 4)	MAX9205	16MHz	23	35	mA
				40MHz	34	45	
			MAX9207	40MHz	32	50	
				66MHz	45	60	
Power-Down Supply Current	I _{CCX}	PWRDN = low				8	mA

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AC ELECTRICAL CHARACTERISTICS

($V_{CC} = +3.0V$ to $+3.6V$, $R_L = 27\Omega \pm 1\%$ or $50\Omega \pm 1\%$, $C_L = 10pF$, $T_A = -40^\circ C$ to $+85^\circ C$. Typical values are at $V_{CC} = +3.3V$ and $T_A = +25^\circ C$, unless otherwise noted.) (Notes 2, 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
TRANSMIT CLOCK (TCLK) TIMING REQUIREMENTS							
TCLK Center Frequency	f_{TCCF}		MAX9205	16	40	MHz	
			MAX9207	40	66	MHz	
TCLK Frequency Variation	TCFV		-200		200	ppm	
TCLK Period	t_{TCP}		MAX9205	25	62.5	ns	
			MAX9207	15.15	25		
TCLK Duty Cycle	TCDC		40		60	%	
TCLK Input Transition Time	t_{CLKT}	Figure 3		3	6	ns	
TCLK Input Jitter	t_{JIT}				150	ps (RMS)	
SWITCHING CHARACTERISTICS							
Low-to-High Transition Time	t_{LHT}	Figure 4	$R_L = 27\Omega$	150	300	400	ps
			$R_L = 50\Omega$	150	350	500	
High-to-Low Transition Time	t_{HLT}	Figure 4	$R_L = 27\Omega$	150	300	400	ps
			$R_L = 50\Omega$	150	350	500	
IN_ Setup to TCLK	t_s	Figure 5	1			ns	
IN_ Hold from TCLK	t_H	Figure 5	3			ns	
OUTPUT High State to High-Impedance Delay	t_{HZ}	Figures 6, 7		4.5	10	ns	
OUTPUT Low State to High-Impedance Delay	t_{LZ}	Figures 6, 7		4.5	10	ns	
OUTPUT High Impedance to High-State Delay	t_{ZH}	Figures 6, 7		4.5	10	ns	
OUTPUT High Impedance to Low-State Delay	t_{ZL}	Figures 6, 7		4.5	10	ns	
SYNC Pulse Width	t_{SPW}		$6 \times t_{TCP}$			ns	
PLL Lock Time	t_{PL}	Figure 7	$2048 \times t_{TCP}$		$2049 \times t_{TCP}$	ns	
Bus LVDS Bit Width	t_{BIT}			$t_{TCP} / 12$		ns	
Serializer Delay	t_{SD}	Figure 8	$t_{TCP} / 6$		$(t_{TCP} / 6) + 5$	ns	

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AC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = +3.0V$ to $+3.6V$, $R_L = 27\Omega \pm 1\%$ or $50\Omega \pm 1\%$, $C_L = 10pF$, $T_A = -40^\circ C$ to $+85^\circ C$. Typical values are at $V_{CC} = +3.3V$ and $T_A = +25^\circ C$, unless otherwise noted.) (Notes 2, 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Deterministic Jitter (Figure 9)	t_{DJIT}	MAX9205	16MHz			200	ps (pk-pk)
			40MHz			140	
		MAX9207	40MHz			140	
			66MHz			140	
Random Jitter (Figure 10)	t_{RJIT}	MAX9205	16MHz			13	ps (RMS)
			40MHz			9	
		MAX9207	40MHz			9	
			66MHz			6	

Note 1: Current into a pin is defined as positive. Current out of a pin is defined as negative. All voltages are referenced to ground except V_{OD} , ΔV_{OD} , and V_{OS} .

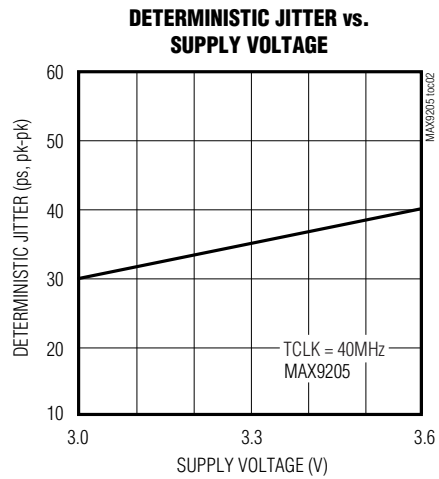
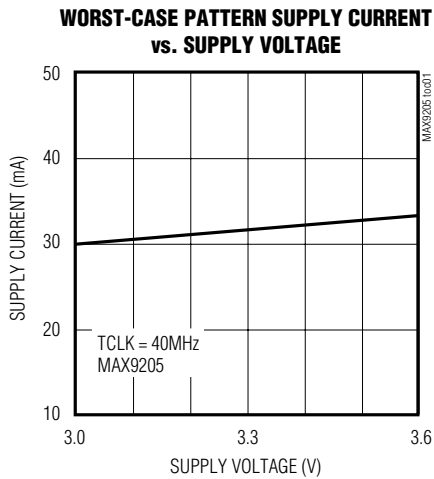
Note 2: C_L includes scope probe and test jig capacitance.

Note 3: Parameters 100% tested at $T_A = +25^\circ C$. Limits over operating temperature range guaranteed by design and characterization.

Note 4: AC parameters are guaranteed by design and characterization.

Typical Operating Characteristics

($V_{CC} = +3.3V$, $R_L = 27\Omega$, $C_L = 10pF$, $T_A = +25^\circ C$, unless otherwise noted.)



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MAX9205/MAX9207

Pin Description

PIN	NAME	FUNCTION
1, 2	SYNC 1, SYNC 2	LVC MOS/LVTTL Logic Inputs. The two SYNC pins are ORed. When at least one of the two pins are asserted high for at least six cycles of TCLK, the serializer initiates a transmission of 1024 SYNC patterns. If held high after 1024 SYNC patterns have been transmitted, SYNC patterns continue to be sent until the SYNC pin is asserted low. Toggling a SYNC pin after six TCLK cycles high and before 1024 SYNC patterns have been transmitted does not affect the output of the 1024 SYNC patterns.
3–12	IN0–IN9	LVC MOS/LVTTL Data Inputs. Data is loaded into a 10-bit latch by the selected TCLK edge.
13	TCLK_R/ \bar{F}	LVC MOS/LVTTL Logic Input. High selects a TCLK rising-edge data strobe. Low selects a TCLK falling-edge data strobe.
14	TCLK	LVC MOS/LVTTL Reference Clock Input. The MAX9205 accepts a 16MHz to 40MHz clock. The MAX9207 accepts a 40MHz to 66MHz clock. TCLK provides a frequency reference to the PLL and strobes parallel data into the input latch.
15, 16	DGND	Digital Circuit Ground. Connect to ground plane.
17, 26	AVCC	Analog Circuit Power Supply (Includes PLL). Bypass AVCC to ground with a 0.1 μ F capacitor and a 0.001 μ F capacitor. Place the 0.001 μ F capacitor closest to AVCC.
18, 20, 23, 25	AGND	Analog Circuit Ground. Connect to ground plane.
19	EN	LVC MOS/LVTTL Logic Input. High enables serial data output. Low puts the bus LVDS output into high impedance.
21	OUT-	Inverting Bus LVDS Differential Output
22	OUT+	Noninverting Bus LVDS Differential Output
24	\bar{PWRDN}	LVC MOS/LVTTL Logic Input. Low puts the device into power-down mode and the output into high impedance.
27, 28	DVCC	Digital Circuit Power Supply. Bypass DVCC to ground with a 0.1 μ F capacitor and a 0.001 μ F capacitor. Place the 0.001 μ F capacitor closest to DVCC.

Detailed Description

The MAX9205/MAX9207 are 10-bit serializers designed to transmit data over balanced media that may be a standard twisted-pair cable or PC board traces at 160Mbps to 660Mbps. The interface may be double-terminated point-to-point or a heavily loaded multipoint bus. The characteristic impedance of the media and connected devices can range from 100 Ω for a point-to-point interface to 54 Ω for a heavily loaded multipoint bus. A double-terminated point-to-point interface uses a 100 Ω -termination resistor at each end of the interface, resulting in a load of 50 Ω . A heavily loaded multipoint bus requires a termination as low as 54 Ω at each end of the bus, resulting in a termination load of 27 Ω . The serializer requires a deserializer such as the MAX9206/MAX9208 for a complete data transmission application.

A high-state start bit and a low-state stop bit, added internally, frame the 10-bit parallel input data and ensure a transition in the serial data stream. Therefore, 12 serial bits are transmitted for each 10-bit parallel input. The MAX9205 accepts a 16MHz to 40MHz reference clock, producing a serial data rate of 192Mbps (12 bits x 16MHz) to 480Mbps (12 bits x 40MHz). The MAX9207 accepts a 40MHz to 66MHz reference clock, producing 480Mbps to 792Mbps. However, since only 10 bits are from input data, the actual throughput is 10 times the TCLK frequency.

To transmit data, the serializers sequence through three modes: initialization mode, synchronization mode, and data transmission mode.

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Initialization Mode

When V_{CC} is applied, the outputs are held in high impedance and internal circuitry is disabled by on-chip power-on-reset circuitry. When V_{CC} reaches 2.35V, the PLL starts to lock to a local reference clock (16MHz to 40MHz for MAX9205 and 40MHz to 66MHz for MAX9207). The reference clock, TCLK, is provided by the system. A serializer locks within 2049 cycles of TCLK. Once locked, a serializer is ready to send data or SYNC patterns depending on the levels of SYNC 1 and SYNC 2.

Synchronization Mode

To rapidly synchronize with a deserializer, SYNC patterns can be sent. A SYNC pattern is six consecutive ones followed by six consecutive zeros repeating every TCLK period. When one or both SYNC inputs are asserted high for at least six cycles of TCLK, the serializer will initiate the transmission of 1024 SYNC patterns. The serializer will continue to send SYNC patterns if either of the SYNC input pins remains high. Toggling one SYNC input with the other SYNC input low before 1024 SYNC patterns are output does not interrupt the output of the 1024 SYNC patterns.

Data Transmission Mode

After initialization, both SYNC input pins must be set low by users or through a control signal from the deserializer before data transmission begins. Provided that SYNC inputs are low, input data at IN0–9 are clocked into the serializer by the TCLK input. Setting TCLK_R/F high selects the rising edge of TCLK for data strobe and low selects the falling edge. If either of the SYNC inputs goes high for six TCLK cycles at any time during

data transmission, the data at IN0–9 are ignored and SYNC patterns are sent for at least 1024 TCLK cycles.

A start bit high and a stop bit low frame the 10-bit data and function as the embedded clock edge in the serial data stream. The serial rate is the TCLK frequency times the data and appended bits. For example, if TCLK is 40MHz, the serial rate is 40×12 (10 + 2 bits) = 480Mbps. Since only 10 bits are from input data, the payload rate is $40 \times 10 = 400$ Mbps.

Power-Down

Power-down mode is entered when the PWRDN pin is driven low. In power-down mode, the PLL of the serializer is stopped and the outputs (OUT+ and OUT-) are in high impedance, disabling drive current and also reducing supply current. When PWRDN is driven high, the serializer must reinitialize and resynchronize before data can be transferred.

High-Impedance State

The serializer output pins (OUT+ and OUT-) are held in high impedance when V_{CC} is first applied and while the PLL is locking to the local reference clock. Setting EN or PWRDN low puts the device in high impedance. After initialization, EN functions asynchronously. For example, the serializer output can be put into high impedance while SYNC patterns are being sent without affecting the internal timing of the SYNC pattern generation. However, if the serializer goes into high impedance, a deserializer loses PLL lock and needs to resynchronize before data transfer can resume.

Table 1. Input /Output Function Table

INPUTS				OUTPUTS
EN	PWRDN	SYNC 1	SYNC 2	OUT+, OUT-
H	H	When either or both SYNC 1 and SYNC 2 are held high for at least six TCLK cycles		Synchronization Mode. SYNC patterns of six 1s and six 0s are transmitted every TCLK cycle for at least 1024 TCLK cycles. Data at IN0–9 are ignored.
H	H	L	L	Data Transmission Mode. IN0–9 and 2 frame bits are transmitted every TCLK cycle.
X	L	X	X	Output in high-impedance.
L	X	X	X	

X = Don't care

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Applications Information

Power-Supply Bypassing

Bypass AVCC with high-frequency surface-mount ceramic 0.1 μ F and 0.001 μ F capacitors in parallel as close to the device as possible, with the smaller valued capacitor closest to AVCC. Bypass DVCC with high-frequency surface-mount ceramic 0.1 μ F and 0.001 μ F capacitors in parallel as close to the device as possible, with the smaller valued capacitor closest to DVCC.

Differential Traces and Termination

Output trace characteristics affect the performance of the MAX9205/MAX9207. Use controlled-impedance media and terminate at both ends of the transmission line in the media's characteristic impedance. Termination with a single resistor at the end of a point-to-point link typically provides acceptable performance. However, the MAX9205/MAX9207 output levels are specified for double-terminated point-to-point and multipoint applications. With a single 100 Ω termination, the output swing is larger.

Avoid the use of unbalanced cables such as ribbon or simple coaxial cable. Balanced cables such as twisted pair offer superior signal quality and tend to generate less EMI due to canceling effects. Balanced cables tend to pick up noise as common mode, which is rejected by a differential receiver.

Eliminate reflections and ensure that noise couples as common mode by running the differential traces close together. Reduce skew by matching the electrical length of the traces. Excessive skew can result in a degradation of magnetic field cancellation.

The differential output signals should be routed close to each other to cancel their external magnetic field. Maintain a constant distance between the differential traces to avoid discontinuities in differential impedance. Avoid 90° turns and minimize the number of vias to further prevent impedance discontinuities.

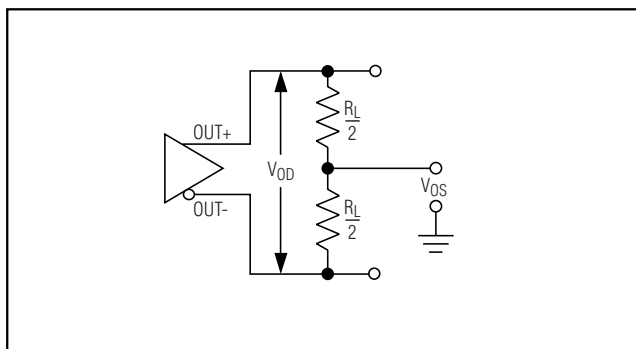


Figure 1. Output Voltage Definitions

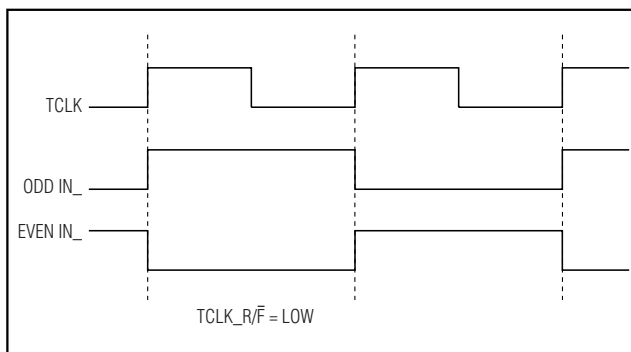


Figure 2. Worst-Case ICC Test Pattern

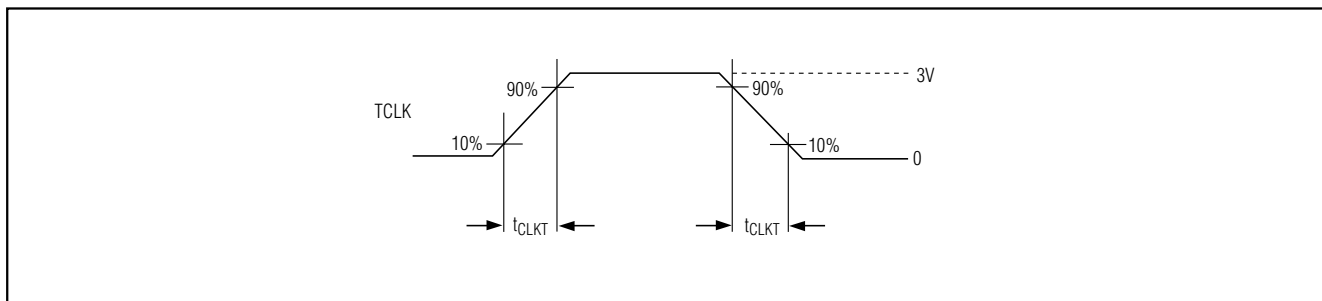


Figure 3. Input Clock Transition Time Requirement

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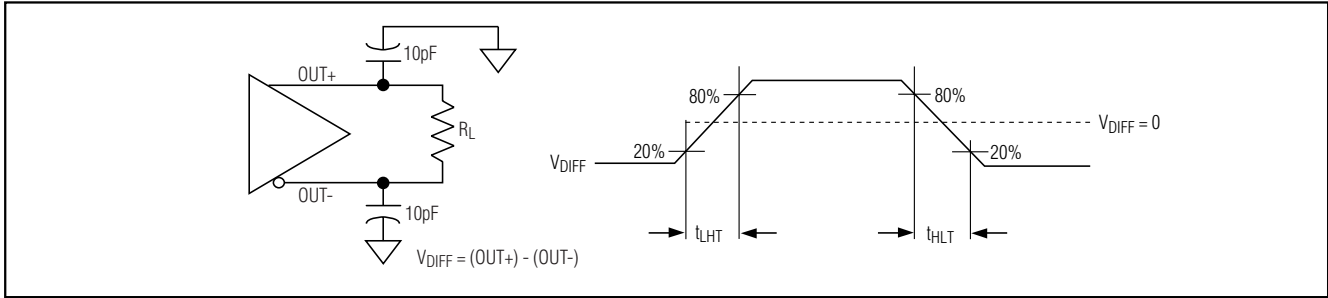


Figure 4. Output Load and Transition Times

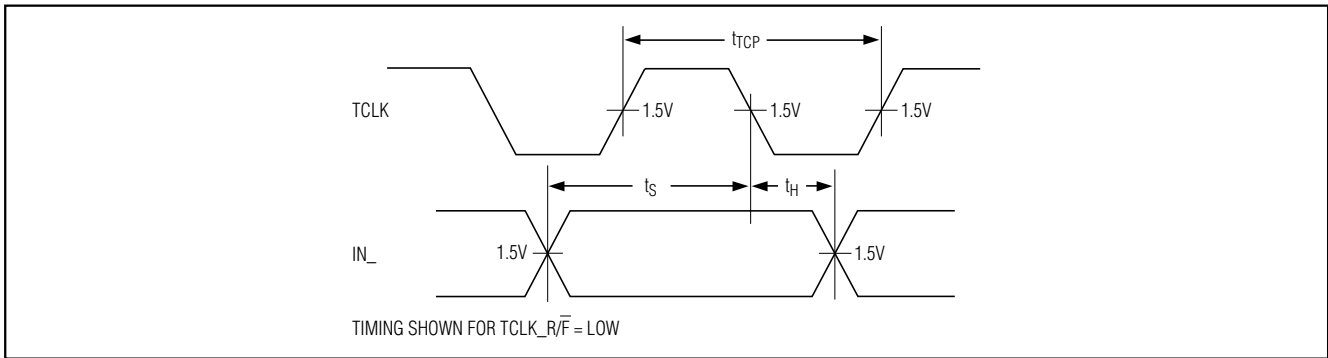


Figure 5. Data Input Setup and Hold Times

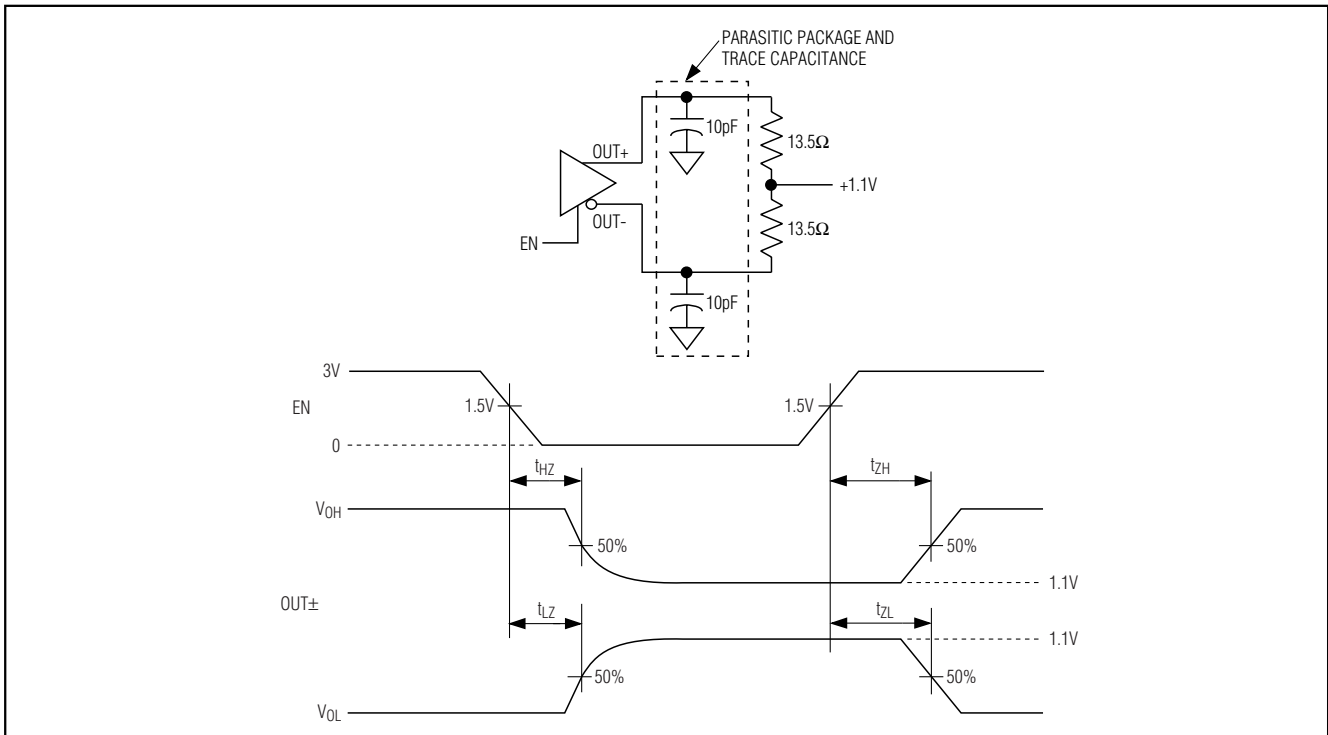


Figure 6. High-Impedance Test Circuit and Timing

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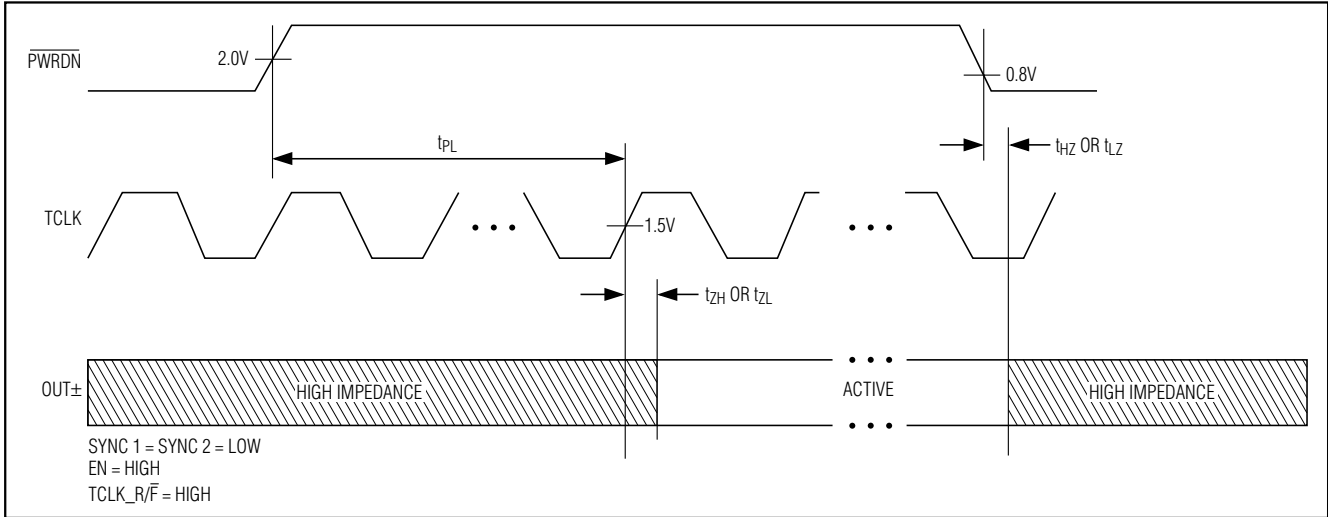


Figure 7. PLL Lock Time and \overline{PWRDN} High-Impedance Delays

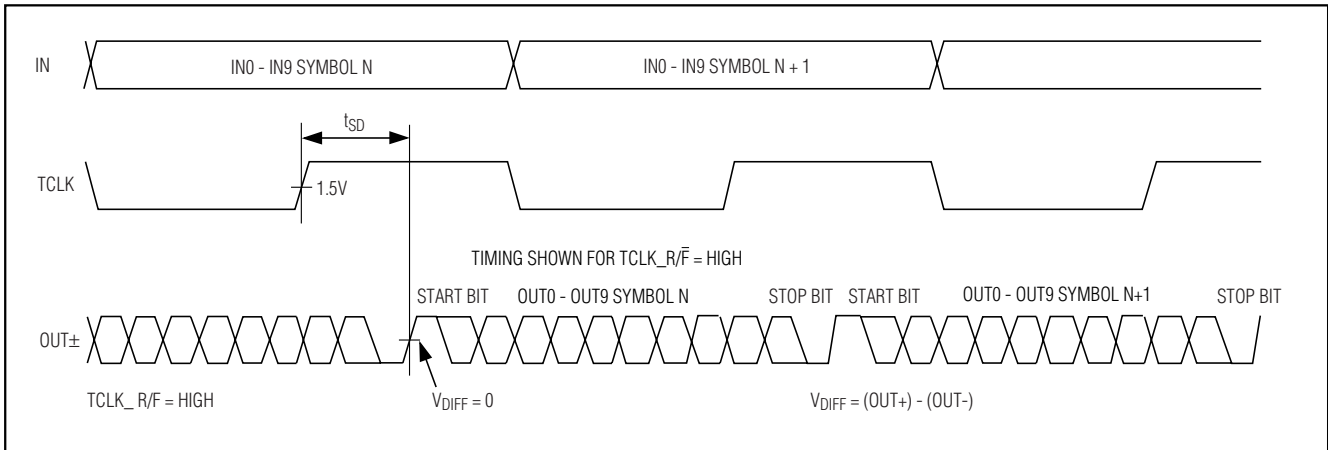


Figure 8. Serializer Delay

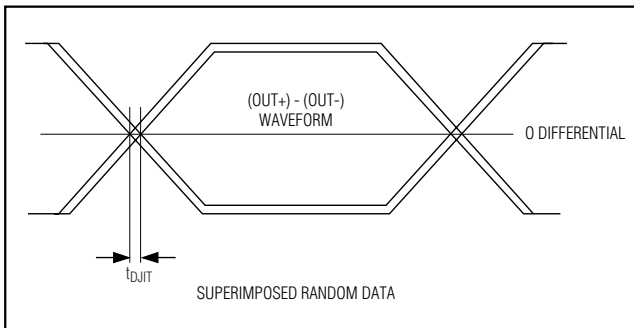


Figure 9. Definition of Deterministic Jitter (t_{DJIT})

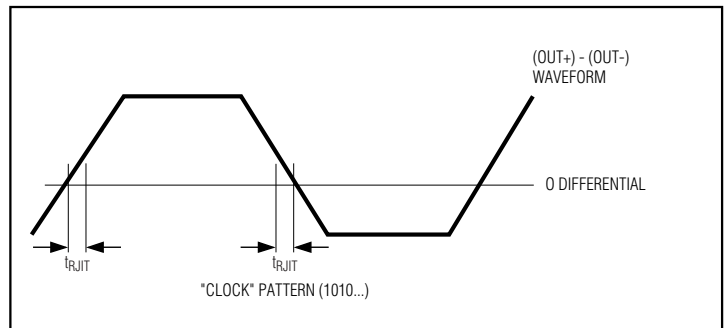


Figure 10. Definition of Random Jitter (t_{RJIT})

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Topologies

The serializers can operate in a variety of topologies. Examples of double-terminated point-to-point, multidrop, point-to-point broadcast, and multipoint topologies are shown in Figures 11 through 14. Use 1% surface-mount termination resistors.

A point-to-point connection terminated at each end in the characteristic impedance of the cable or PC board traces is shown in Figure 11. The total load seen by the serializer is 50Ω. The double termination typically

reduces reflections compared to a single 100Ω termination. A single 100Ω termination at the deserializer input is feasible and will make the differential signal swing larger.

A serializer located at one end of a backplane bus driving multiple deserializers in a multidrop configuration is shown in Figure 12. A 54Ω resistor at the far end terminates the bus. This topology allows “broadcast” of data with a minimum of interconnect.

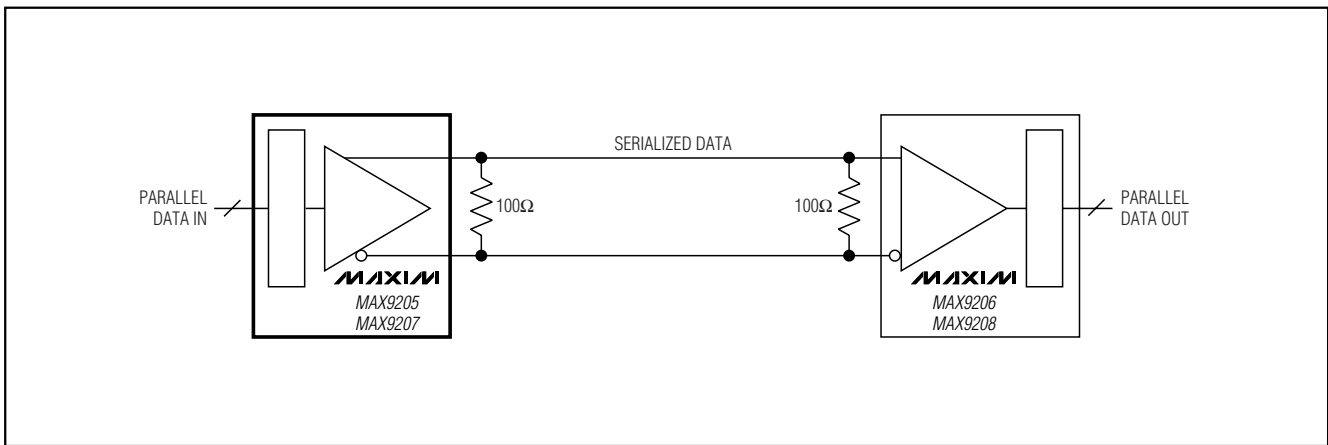


Figure 11. Double-Terminated Point-to-Point

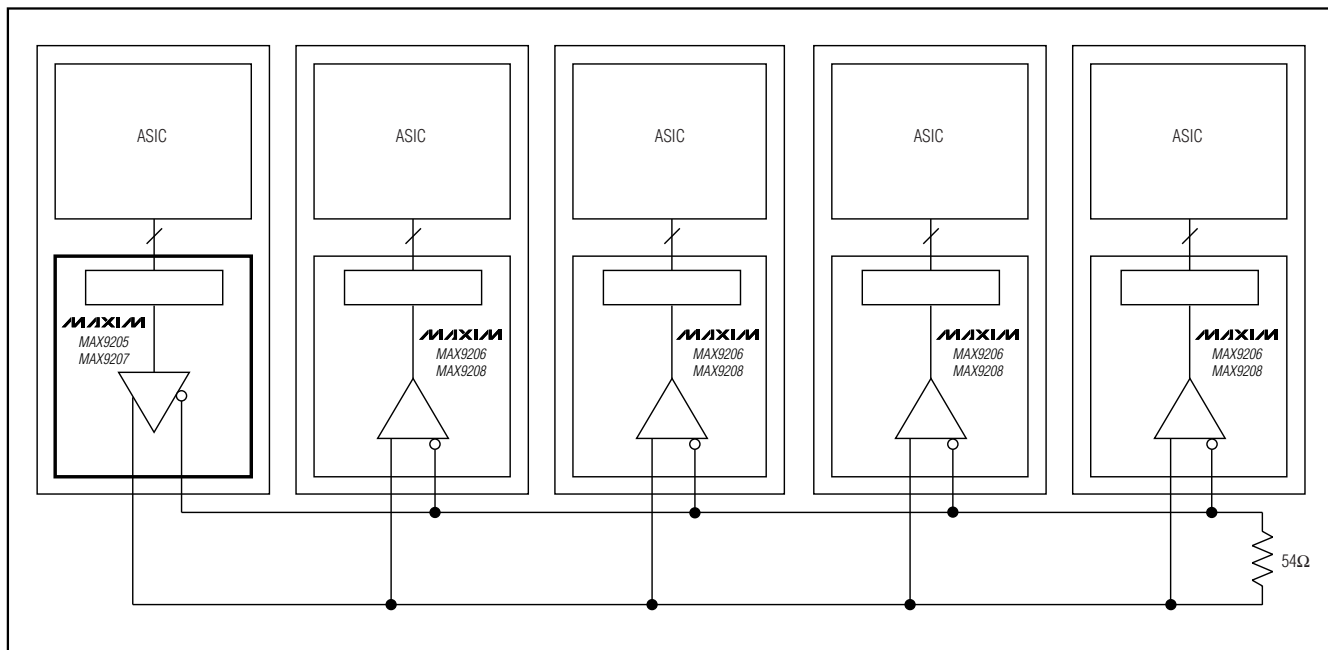


Figure 12. Multidrop

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A point-to-point version of the multidrop bus is shown in Figure 13. The low-jitter MAX9150 10-port repeater is used to reproduce and transmit the serializer output over 10 double-terminated point-to-point links. Compared to the multidrop bus, more interconnect is traded for more robust hot-plug capability.

The repeater eliminates nine serializers compared to 10 individual point-to-point serializer-to-deserializer connections. Since repeater jitter subtracts from the serializer-deserializer timing margin, a low-jitter repeater is essential in most high data rate applications.

Multiple serializers and deserializers based over a differential serial connection on a backplane are shown in Figure 14. The second serializer can be a backup to

the primary serializer. The typical close spacing (1in or less) of cards on a backplane reduces the characteristic impedance by as much as half the initial, unloaded value. Termination resistors that match the loaded characteristic impedance are required at each end of the bus. The total loaded seen by the serializer is 27Ω in this case.

Board Layout

For bus LVDS applications, a four-layer PC board that provides separate power, ground, and input/output signals is recommended. Separate LVTTTL/LVCMOS and bus LVDS signals from each other to prevent coupling into the bus LVDS lines.

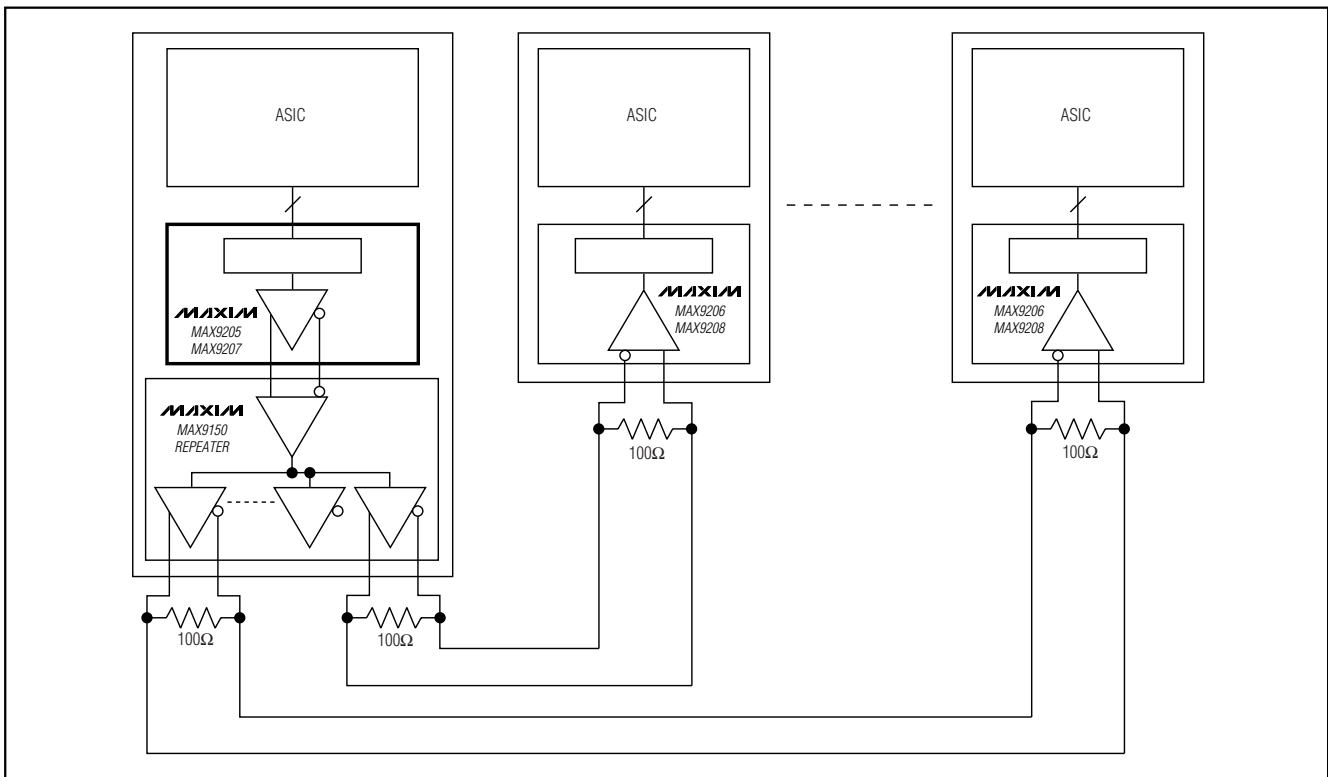


Figure 13. Point-to-Point Broadcast Using MAX9150 Repeater

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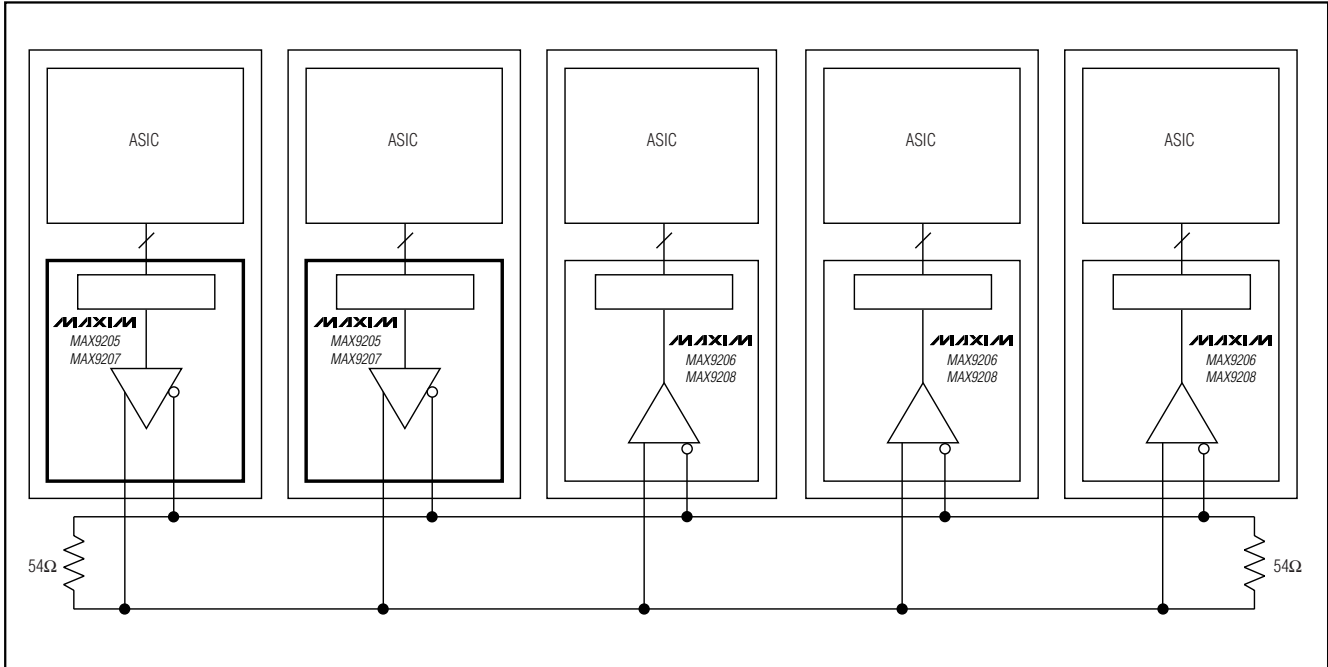
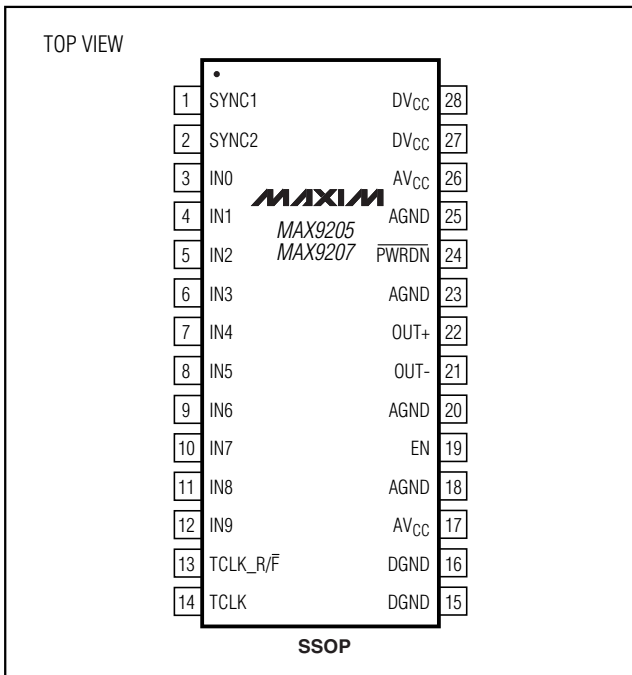
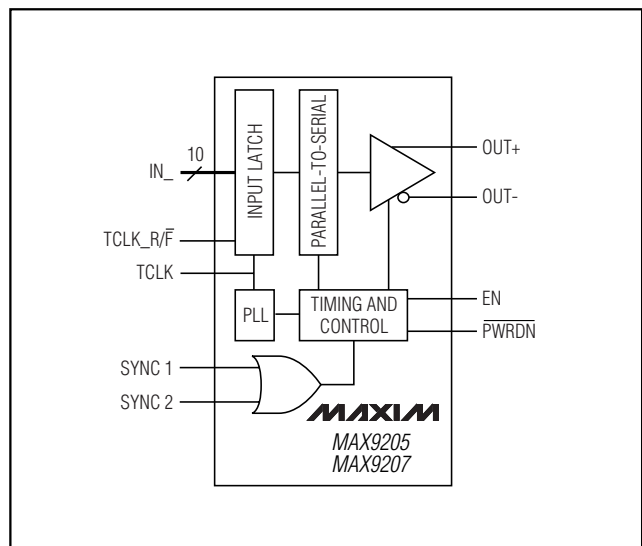


Figure 14. Multipoint

Pin Configuration



Functional Diagram



Chip Information

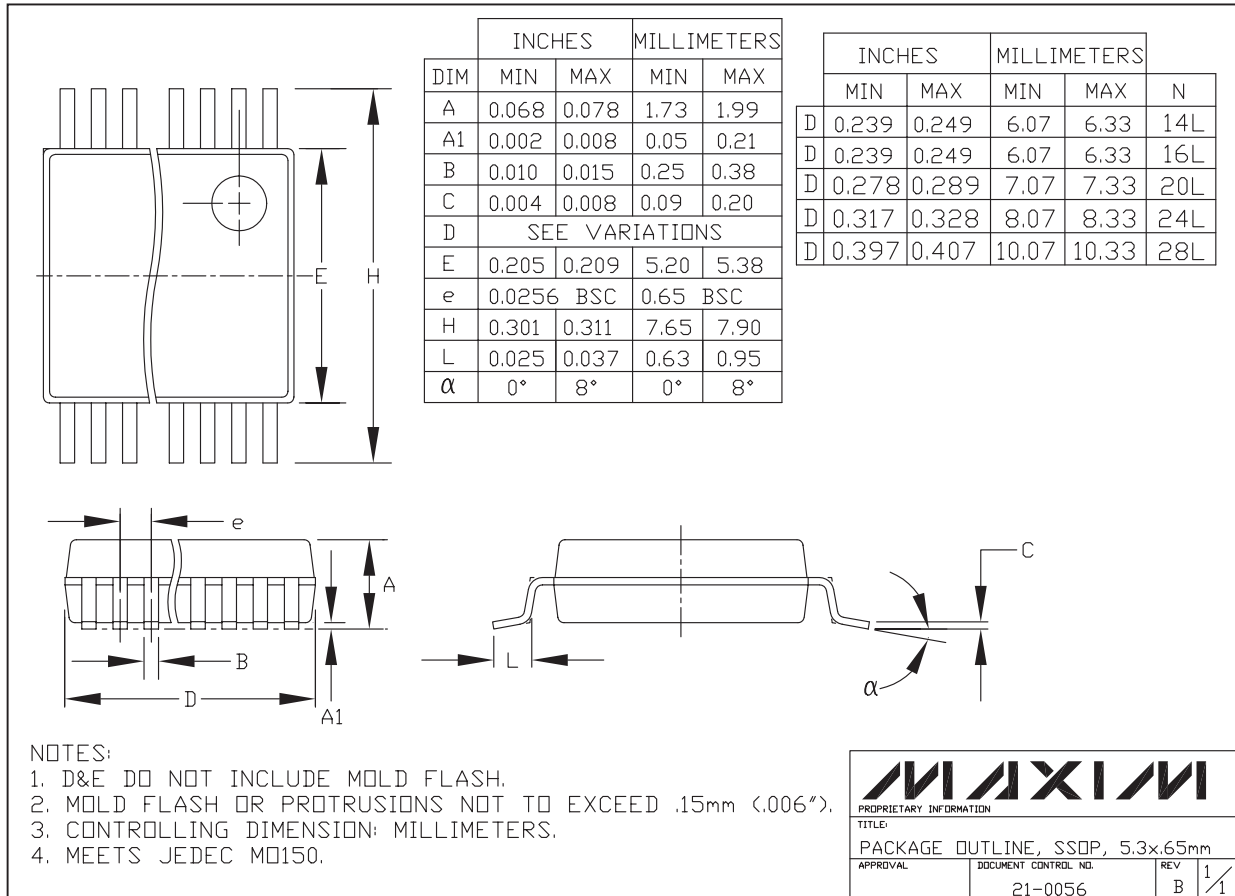
TRANSISTOR COUNT: 3036

PROCESS: CMOS

10-Bit Bus LVDS Serializers

Package Information

MAX9205/MAX9207



SSOP(EPS)

MAXIM			
PROPRIETARY INFORMATION			
TITLE: PACKAGE OUTLINE, SSOP, 5.3x.65mm			
APPROVAL	DOCUMENT CONTROL NO.	REV	1/1
	21-0056	B	

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